Remarks

Receipt is acknowledged of the Office Action mailed May 20, 2004. Claims 1-8 were pending in the application. Claims 1-5 and 8 were elected for prosecution per the Restriction Requirement of April 2, 2004. Thus, claims 6 and 7 have been cancelled as pertaining to a non-elected group. Further, claims 1 and 3-5 have been amended to more fully recite features of the present invention. No new matter has been introduced. As such, claims 1-5 and 8 are submitted for reconsideration at this time.

Rejections under 35 U.S.C § 102(b)

Claims 1 and 2 stand rejected under 35 U.S.C § 102(b) as being anticipated by U.S. Patent No. 5,594,361 ("Campbell 1" hereafter). Claim 1 also stands rejected under 35 U.S.C § 102(b) as being anticipated by U.S. Patent No. 6,060,926 ("Campbell 2" hereafter). Applicant respectfully traverses the rejections under 35 U.S.C § 102(b) for at least the following reasons.

U.S. Patent No. 5,594,361 (Campbell 1)

As set forth on page 2 of the pending Office Action, Campbell 1 allegedly discloses in Figure 7 a first time hysteresis unit 71 and a second time hysteresis unit 73. Figure 7 is reproduced below for the Examiner's convenience.

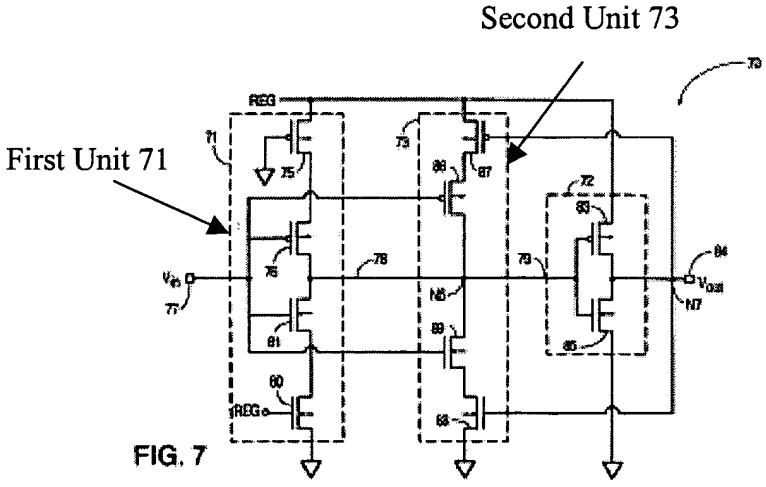


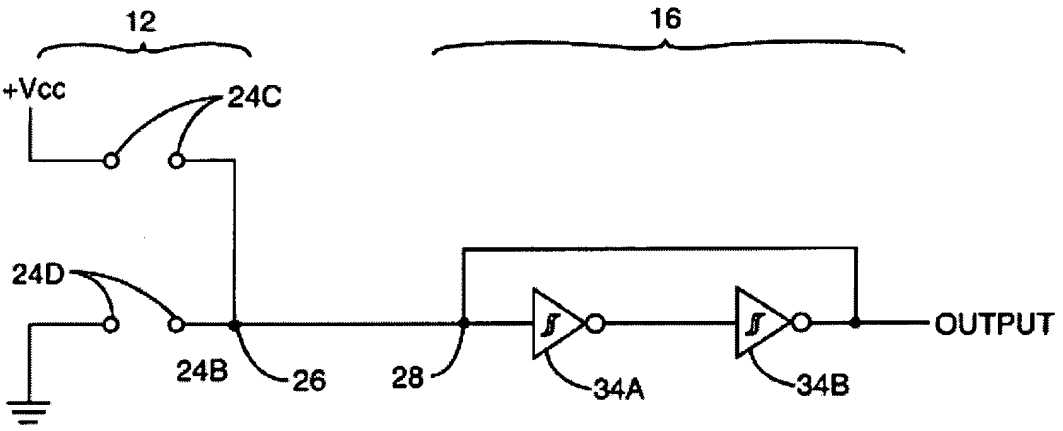
FIG. 7

As shown above, the first time hysteresis unit 71 and second time hysteresis unit 73 of Campbell 1 are connected *in parallel*. Thus, the first time hysteresis unit 71 and the second time

hysteresis unit 73 of Campbell 1 are not connected *in series* as recited in the originally filed claim 1. As Campbell 1 fails to disclose or suggest the claimed series configuration, Campbell 1 cannot anticipate the claimed invention as originally filed.

U.S. Patent No. 6,060,926 (Campbell 2)

As set forth on page 3 of the Office Action, Campbell 2 allegedly discloses in Figure 4 a pulse conditioning circuit including a first time hysteresis unit 34A in series connection with a second time hysteresis unit 34B. Figure 4 of Campbell 2 is provided below for the Examiner's convenience.



The presently claimed invention recites a hysteresis circuit including a first time hysteresis unit and a second time hysteresis unit to minimize glitches by latching an input signal for a predetermined time in a serially connected latch structure when a glitch is generated in the input signal. In this regard, the presently claimed invention recites a delay unit for setting a latch time of the first time hysteresis unit to be different from that of the second time hysteresis unit. In particular, the presently claimed invention recites the second time hysteresis unit latching the input signal for a predetermined time of a second delay *longer than* the first delay, which optimizes the delay for the given transition (high to low or low to high). No such configuration is disclosed or suggested by Campbell 2.

Specifically, Campbell 2 discloses a latch circuit 16 (col. 4, line 6) including two series inverters with hysteresis 34A, 34B (col. 4, lines 21-24). The two series inverters provide an exact output signal when a glitch is generated in an input signal. As such, the two series inverters in Campbell 2 do not latch the input signal for a different predetermined time based on

whether the transition is high to low or low to high as claimed. Thus, Campbell 2 fails to anticipate the presently claimed invention.

Conclusion

Thus, for at least the aforementioned reasons, Applicant submits that claims 1 and 2 are not anticipated by the presently cited art. Withdrawal of the rejections under 35 U.S.C. § 102(b) is solicited.

Rejections under 35 U.S.C § 103(a)

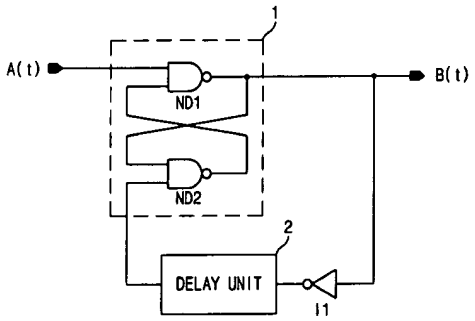
Claims 2-5 and 8 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Campbell 2 in view of the prior art depicted by Applicant's Figure 1. Claims 2-5 and 8 are dependent upon independent claim 1, and are believed to be allowable for at least the aforementioned reasons with respect to claim 1. Applicant further submits that claims 2-5 and 8 are allowable for the following additional reasons.

The Office Action acknowledges on page 3 that Campbell 2 fails to disclose "[the details of] 'an inverter' (claim 2); the details of the 'first time hysteresis unit' and 'the second time hysteresis unit' (claims 3-4); [and] 'second delay time is more than two times longer than the first delay time' (claims 5 and 8)." The Office Action asserts, however, that inverters are old and notoriously well known in the art, and that it would have been obvious at the time the invention was made for one skilled in the art to incorporate an inverter to the output for buffering or level inverting purposes. The Office Action further asserts that Applicant's Figure 1 discloses the detail of a conventional time hysteresis unit, and that it would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ Figure 1 unit in Campbell 2, since this allegedly involves nothing more than showing the details of what might typically comprise the first or second time hysteresis unit of Campbell 2. Finally, the Office Action asserts that the limitation "second delay time is more than two times longer than the first delay time" is not of patentable merit because it is notoriously well known in the art that different values for the delay time can be selected in order to produce correspondingly different output values. Applicant respectfully traverses these assertions as discussed in greater detail below.

In the presently claimed invention, glitches generated in an input signal transitioning from "1" to "0" are addressed by a first time hysteresis unit, which delays the input signal for a delay time td1 to output an output signal substantially without glitches. Further, in regards to glitches

generated in an input signal transitioning from "0" to "1", the second time hysteresis unit delays the output signal from the first time hysteresis unit for a delay time td2 to output an output signal substantially without glitches. The second delay time td2 is set to be longer than the first delay time td1 in order to optimize the glitch removing capability of the present invention. Applicant has amended claim 1 to more fully recite this feature. No such feature is disclosed or suggested in the prior art.

As shown in Figure 1 (reproduced below for the Examiner's convenience), the prior art circuit includes a latch 1 connected in series with inverter I1 and delay unit 2.



As acknowledged by the Office Action, the delay unit in Figure 1 does not delay the transition at a different time as claimed. However, the Examiner asserts that "it is known in the art that different values for the delay time can be selected in order to produce correspondingly different output values." Applicant respectfully disagrees with this assertion as it pertains to claims 2-5 and 8.

Without acquiescing to the Examiner's assertion, even if it is known that a different delay value results in a different output value, this still does not demonstrate it was known in the art to vary the delay amount *based on whether the transition was from the first to second level, or from the second to first level* as claimed (e.g., "0" to "1" and "1" to "0"), or in an amount where the second delay time is more than two times longer than the first delay time as claimed. In order words, simply knowing that varying the delay amount results in a corresponding delayed output value does not demonstrate varying the delay amount in the claimed manner to achieve the claimed result. To the extent the Examiner makes such an assertion, Applicant respectfully requests that the Examiner provide a reference as required under MPEP §2144.03 (If the applicant traverses such an assertion the examiner should cite a reference in support of his or her position).

Applicant further submits that there is no motivation within either cited reference for one of ordinary skill in the art to combine the two references in such away as to achieve the presently claimed invention. Specifically, in view of the substantial differences between Applicant's Figure 1 (one delay unit) and Campbell 2 (two delay inverters) combining the two references would materially alter operation of the two references. As set forth in MPEP §2143.01, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious. Thus, the motivation relied upon must be based on improper hindsight reasoning gleaned only from Applicant's disclosure. See MPEP §2145(X)(A) (Impermissible Hindsight).

In view of the aforementioned arguments, Applicant respectfully submits that claims 2-5 and 8 are allowable over the cited art. Withdrawal of the rejection under 35 U.S.C. §103(a) is solicited.

CONCLUSION

In view of the above amendment and remarks, Applicant respectfully requests that all objections and rejections be withdrawn and that a notice of allowance be forthcoming. The Examiner is invited to contact the undersigned for any reason related to the advancement of this case.

Respectfully submitted,

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